

1 CLAIM LISTING

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3 1. (Currently amended) A substrate with a via and pad structure [[for]]  
4 connecting a surface mount component to conductive layers of the substrate,  
5 comprising:  
6 a surface mount component, wherein the surface mount component includes a  
7 package having an upper surface with solderable terminal sides and a terminal end; [[.]]  
8 comprising:  
9 a substrate;  
10 a plated via connected to the conductive layers;  
11 a solder mask surrounding the plated via; and  
12 a conductive pad with a conductive trace connected to the plated via, wherein the  
13 solder mask exposes a part of the conductive pad that extends beyond the solderable  
14 terminal sides of the surface mount component to increase solder formation between  
15 the conductive pad and the solderable terminal sides and to reduce solder formation at  
16 the first plated via.  
17

18 2. (Currently amended) The substrate with the via and pad structure of claim  
19 1, wherein the solder mask covers a part of the conductive pad that extends beyond the  
20 solderable terminal end and reduces solder formation at the terminal end of the surface  
21 mount component.  
22

23 3. (Previously presented) The substrate with the via and pad structure of  
24 claim 2, wherein the conductive pad includes a first arm and a second arm that extend  
25 beyond the solderable terminal sides of the surface mount component.  
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27 4. (Original) The substrate with the via and pad structure of claim 3, wherein  
28 the first arm and the second arm are symmetrically disposed on the substrate with  
29 respect to the plated via.  
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1           5.     (Original) The substrate with the via and pad structure of claim 2, wherein  
2     the conductive pad includes a first arm, a second arm, and a body.

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4           6.     (Original) The substrate with the via and pad structure of claim 5, wherein  
5     the first arm and the second arm are symmetrically disposed on the substrate with  
6     respect to the plated via.

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8           7.     (Original) The substrate with the via and pad structure of claim 2, wherein  
9     the conductive pad includes a T-shirt shaped structure.

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11          8.     (Original) The substrate with the via and pad structure of claim 7, wherein  
12     the T-shirt shaped structure is symmetrically disposed on the substrate with respect to  
13     the plated via.

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15          9.     (Original) The substrate with the via and pad structure of claim 2, wherein  
16     the solder mask is keyhole shaped.

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18          10.    (Original) The substrate with the via and pad structure of claim 2, wherein  
19     the solder mask covers the substrate partially or entirely except the conductive pad and  
20     the plated via.

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22          11.    (Previously presented) The substrate with the via and pad structure of  
23     claim 2, further comprising a surface mount component electrically connected to the  
24     conductive pad through solder joint(s), wherein the solder joints have a greater volume  
25     at the solderable terminal sides than at the terminal end of the surface mount  
26     component.

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28          12.    (Original) The substrate with the via and pad structure of claim 2, wherein  
29     the substrate is part of a printed circuit board.  
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1        13. (Previously presented) The substrate with the via and pad structure of  
2 claim 2, wherein the substrate is part of a BGA package footprint.

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4        14. (Currently amended) A substrate with a plurality of via and pad structures  
5 ~~[[for]]~~ connecting a surface mount component to conductive layers of the substrate,  
6 comprising:

7        a surface mount component, wherein the surface mount component includes a  
8 package having an upper surface with first solderable terminal sides and a first terminal  
9 end and second solderable terminal sides and a second terminal end ~~[[,]]~~ comprising:

10        a substrate;

11        a first plated via connected to the conductive layers;

12        a first solder mask surrounding the first plated via;

13        a second plated via connected to an associated conductive layer;

14        a second solder mask surrounding the second plated via;

15        a first conductive pad with a conductive trace connected to the first plated via,  
16 wherein the first conductive pad includes a portion that is exposed to solder and  
17 extends beyond the first solderable terminal sides of the surface mount component to  
18 increase solder formation along the first solderable terminal sides and to reduce solder  
19 formation at the first plated via; and

20        a second conductive pad with a conductive trace connected to the second plated  
21 via, wherein the second conductive pad includes a portion that is exposed to solder and  
22 extends beyond the second solderable terminal sides of the surface mount component  
23 to increase solder formation along the second solderable terminal sides and to reduce  
24 solder formation at the second plated via.

25        15. (Previously presented) The substrate with the plurality of via and pad  
26 structures of claim 14, wherein the first solder mask covers and reduces solder  
27 formation at the first terminal end of the surface mount component and the second  
28 solder mask covers and reduces solder formation at the second terminal end of the  
29 surface mount component.  
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1        16.    (Previously presented) The substrate with the plurality of via and pad  
2 structures of claim 15, wherein each of the first and second conductive pads include a  
3 first arm and a second arm.

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5        17.    (Original) The substrate with the plurality of via and pad structures of claim  
6 16, wherein each of the first and second conductive pads is symmetric to the first plated  
7 via and the second plated vias, respectively.

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9        18.    (Original) The substrate with the plurality of via and pad structures of  
10 claim 15, wherein the first and second conductive pads include a first arm, a second  
11 arm, and a body.

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13       19.    (Original) The substrate with the plurality of via and pad structures of claim  
14 18, wherein each of the first and second conductive pads is symmetric to the first plated  
15 via and the second plated vias, respectively.

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17       20.    (Original) The substrate with the plurality of via and pad structures of claim  
18 15, wherein each of the first and second conductive pads include a T-shirt shaped  
19 structure.

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21       21.    (Original) The substrate with the plurality of via and pad structures of claim  
22 20, wherein each of the T-shirt shaped structures is symmetric to the first and second  
23 plated vias, respectively.

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25       22.    (Original) The substrate with the plurality of via and pad structures of claim  
26 15, wherein each of the first and second solder masks is a ring surrounding the first and  
27 second plated vias, respectively.

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29       23.    (Original) The substrate with the plurality of via and pad structures of claim  
30 15, wherein each of the first and second solder masks is a keyhole shape and  
surrounds the first and second plated vias, respectively.

1        24. (Original) The substrate with the plurality of via and pad structures of claim  
2 15, wherein each of the first and second solder masks cover the substrate partially or  
3 entirely except the first and second conductive pads and the first and second plated  
4 vias.

5  
6        25. (Previously presented) The substrate with the plurality of via and pad  
7 structures of claim 15, further comprising a surface mount component electrically  
8 connected to the first and second conductive pads through solder joint(s), wherein the  
9 solder joint(s) have a greater volume at each of the solderable terminal sides than at  
10 each terminal end of the surface mount component.

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12        26. (Previously presented) The substrate with the plurality of via and pad  
13 structures of claim 15, wherein the separation along the substrate between the first and  
14 second solder masks defines the length of the surface mount component to be  
15 soldered.

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17        27. (Original) The substrate with the plurality of via and pad structures of claim  
18 15, wherein the substrate is part of a printed circuit board.

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20        28. (Previously presented) The substrate with the plurality of via and pad  
21 structures of claim 15, wherein the substrate is part of a BGA package footprint.

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23        29. (Original) The substrate with the via and pad structure of claim 2, wherein  
24 solder mask is a ring surrounding the plated via.

25        30. (Withdrawn) A method of reducing solder wicking on a substrate with  
26 associated conductive layers, comprising:  
27        (a) forming a via and pad structure;  
28        (b) masking around the plated via to reduce solder formation at the plated via;  
29        (c) placing a component having terminal sides and a terminal end on the  
30 conductive pad;

1 (d) extending the conductive pad beyond the terminal sides of the component to  
2 increase solder formation along the terminal sides; and

3 (e) soldering the component to the conductive pad.  
4

5 31. (Withdrawn) The method of claim 30, further comprising repeating steps  
6 (a) through (e) for a plurality of via and pad structures.  
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8 32. (Withdrawn) The method of claim 30, wherein the conductive pad is a T-  
9 shirt shaped structure.  
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11 33. (Withdrawn) The method of claim 31, wherein the masking around plated  
12 via is accomplished by a keyhole shaped structure.  
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14 34. (Original) The substrate with the plurality of via and pad structures of claim  
15 14, wherein the first conductive pad extends beyond the terminal side of the component  
16 a maximum distance that reduces solder wicking without generating electrical shorts  
17 between the first conductive pad and an adjacent plated via.  
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19 35. (Withdrawn) A computer implemented method for calculating the  
20 maximum distance of a conductive pad extending beyond the terminal side of a  
21 component, wherein the component is placed diagonally in an array of four plated vias,  
22 comprising:

23 (a) storing L1 representing the center-to-center distance of a first plated via and a  
24 second plated via;

25 (b) storing L3 representing the length and L4 the width of the component;

26 (c) storing L5 representing the length of the conductive pad extending beyond the  
27 terminal side;

28 (d) storing R representing an outer radius of a first plated via;

29 (e) storing X representing the minimum distance between the first plated via and  
30 the conductive pad;

1 (f) calculating L2, representing the center-to-center distance between the first  
2 plated via and a third plated via, by dividing L1 by  $\sin 45^\circ$ ;

3 (g) calculating L8, representing the distance from the center of the first plated via  
4 to the side of the component, by subtracting L4 from L2 and dividing by two;

5 (h) calculating L7, representing half the distance between the conductive pad and  
6 an opposite conductive pad, by dividing L3 by two and subtracting L5;

7 (i) calculating L11 by summing R and X;

8 (j) calculating L9 by taking the square root of the difference of the square of L11  
9 and the square of L7; and

10 (k) calculating L10 by subtracting L9 from L8, wherein L10 is the maximum  
11 distance of the conductive pad extending beyond the terminal side of the component.